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10/725,129	12/01/2003	Takeshi Yamazaki	SCEI 3.0-155	2626

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EXAMINER	
CAMPOS, YAIMA	
ART UNIT	PAPER NUMBER
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/725,129	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/725,129 has a total of 29 claims pending in the application; there are 5 independent claims and 24 dependent claims, all of which are ready for examination by the examiner.

2. This Non-Final Office action results from examination and search of claims 1-29 of the instant application. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Patent Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

IV. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

5. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated July 5, 2005 is acknowledged by the examiner and the cited

references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 12 and 19-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Stone et al. (US 5,742,785).

8. As per **claim 12**, Stone discloses a system, comprising:

a shared memory; **["shared memory locations 28" (Figure 1)]**

a memory interface unit coupled to the shared memory and operable to retrieve data from the shared memory at requested addresses, and to write data to the shared memory at requested addresses; **["interconnection network 20" (Figure 1 and related text) "read the share-memory locations, modify their contents, and then write back the new values atomically" (Col. 6, lines 54-62)]**

and a plurality of processing units in communication with the memory interface and operable to instruct the memory interface unit that data be loaded with reservation from the shared memory at a specified address such that any operations may be performed on the data, wherein at least

one of the processing units includes a status register having one or more bits indicating whether a reservation was lost, the reservation being lost when the data at the specified address in shared memory is modified by another one or more of the processing units [**"Load-with-Reservation" (Col. 9, line 54-Col. 10, line 35) "plurality of processors (block 21)... each processor is composed of the blocks shown within block 21... The ResReg[j].S 34 field is typically a 1-bit status flag that indicates whether or not the reservation register 30 holds a reservation... the shared memory location 28 is associated with the register when the location 28 address is stored in the reservation register 30 ResReg[j]." (Col. 8, line 28-Col. 9, lines 3-6; Figure 1 and related text) and explains "a remote processor or process modifies (writes to) a reserved shared variable, and invalidates a reservation" (Col. 10, lines 36-55)**].

9. As per **claims 19 and 20**, Stone discloses the system of claim 12, wherein the memory interface unit is operable to monitor whether the reservation is lost by monitoring whether the data at the specified address in shared memory is modified by another of the processing units; wherein the memory interface unit is operable to cause the one or more bits of the status register of the at least one processing unit to indicate that the reservation was lost [**"The test reservations logic in block 61 verifies that the S bit of all selected reservations is 1, signifying that all reservations remain valid. If a remote processor writes a new value to a reserved variable, that action will be communicated to this processor through a cache coherence message, and the action will invalidate the reservation by changing the S bit to 0" (Col. 12, lines 26-46) "TEST RESERVATIONS" (Col. 12, lines 26-46)**].

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 1-11, 13-18 and 21-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. (US 5,742,785) in view of Nieuwland et al. (US 2002/0083276).

12. As per **claims 1, 8 and 21**, Stone discloses a method, comprising:

a shared memory; **["shared memory locations 28" (Figure 1)]**

a memory interface unit coupled to the shared memory and operable to retrieve data from the shared memory at requested addresses, and to write data to the shared memory at requested addresses; **["interconnection network 20" (Figure 1 and related text) "read the share-memory locations, modify their contents, and then write back the new values atomically" (Col. 6, lines 54-62)]**

and a plurality of processing units in communication with the memory interface and operable to instruct the memory interface unit that data be loaded with reservation from the shared memory at a specified address such that any operations may be performed on the data, wherein at least one of the processing units includes a status register having one or more bits indicating whether a reservation was lost, the reservation being lost when the data at the specified address in shared memory is modified by another one or more of the processing units **["Load-with-Reservation" (Col. 9, line 54-Col. 10, line 35) "plurality of processors (block 21)... each processor is**

composed of the blocks shown within block 21... The ResReg[j].S 34 field is typically a 1-bit status flag that indicates whether or not the reservation register 30 holds a reservation... the shared memory location 28 is associated with the register when the location 28 address is stored in the reservation register 30 ResReg[j]." (Col. 8, line 28-Col. 9, lines 3-6; Figure 1 and related text) and explains "a remote processor or process modifies (writes to) a reserved shared variable, and invalidates a reservation" (Col. 10, lines 36-55)].

a) issuing a load with reservation instruction including a requested address to a shared memory at which data may be located; as **["Load-with-Reservation" (Col. 9, line 54-Col. 10, line 35)]**

b) receiving the data from the shared memory such that any operations may be performed on the data; **["store contingent (sc): This instruction places a modified result value in a field of a reservation register associated with a shared memory location in preparation for an atomic update" (Col. 9, lines 57-60)]**

c) at least one of: (i) entering a low power consumption mode, and (ii) initiating another processing task; and **["Write-if-reserved (WR): This instruction performs the atomic update of share memory locations whose addresses are held in reservation registers with valid contents, that have been updated by a Store Contingent instruction after placing the reservation. The atomic update occurs provided that all reservations are valid and write privilege has been obtained successfully for all reservations" (Col. 9, line 62-Col. 10, line 1)]**

d) receiving notification that the reservation was lost, the reservation being lost when the data at the address in shared memory is modified **["a remote processor or process modifies (writes to) a reserved shared variable, and invalidates a reservation" (Col. 10, lines 36-55)]**.

Stone does not explicitly disclose the details of "entering a low power consumption mode."

Nieuwland discloses "entering a low power consumption mode" as **["whenever a station has to wait for the availability of data or buffer space, respectively, it may poll the remote semaphore to see whether the status of the buffer has changed. To prevent the need for polling and the associated bus load and power waste, an interrupt is provided for the consuming (producing) station by the producing (consuming) station after it has changed its own semaphore... Generally, a station may go into low-power mode whenever it has to wait for completion of the accessing by another station. Receiving an interrupt will wake up the idle station and will cause it to re-evaluate the semaphore that had caused the idle state" (Page 2, Par. 0014)]**.

Stone et al. (US 5,742,785) in view of Nieuwland et al. (US 2002/0083276) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the shared memory system which waits to receive a write privilege in order to write into a reserved register as taught by Stone and further have the waiting processor "entering a low power consumption mode" as taught by Nieuwland.

The motivation for doing so would have been because Nieuwland discloses entering a low power consumption mode is done to **[save power (Page 2, Par. 0014)]**.

Therefore, it would have been obvious to combine Stone et al. (US 5,742,785) with Nieuwland et al. (US 2002/0083276) for the benefit of creating a shared memory system to obtain the invention as specified in claims 1, 8 and 21.

13. As per **claims 2 and 9**, the combination of Stone and Nieuwland discloses the method of claim 1, wherein the notification that the reservation was lost operates as an interrupt that at least one of (i) interrupts the low power consumption mode; and (ii) interrupts the other processing task **[Stone discloses "if an invalidate request 104 is received, the invalidate is performed immediately" (Col. 14, lines 8-10) wherein "the invalidate process appears... it sets the S bit of the matching reservation register to 0, and this will prevent the success of a current or subsequent Write-If-Reserved instruction. The invalidate signifies that a variable has changed value or will change value in the immediate future" (Col. 14, lines 38-48). Nieuwland (Page 2, Par. 0014)]**.

14. As per **claims 3 and 10**, the combination of Stone and Nieuwland discloses the method of claim 1, wherein the step of entering the low power consumption mode or the step of initiating another processing task is carried out only if the data is not a predetermined value **[Stone discloses "The test reservations logic in block 61 verifies that the S bit of all selected reservations is 1, signifying that all reservations remain valid. If a remote processor writes a new value to a reserved variable, that action will be communicated to this processor through a cache coherence message, and the action will invalidate the reservation by changing the S bit to 0" (Col. 12, lines 26-46). Nieuwland discloses "semaphore 100 is used to determine which of the stations get preference" (Page 1, Par. 0011; Page 2, Par. 0014)]**.

15. As per **claims 4 and 11**, the combination of Stone and Nieuwland discloses the method of claim 3, further comprising repeating steps a) through d) when the notification indicates that the reservation was lost **[Stone discloses "a message from a remote processor can arrive and invalidate a selected reservation. Therefore, the selected reservations are tested repeatedly" (Col. 12, lines 43-46). Nieuwland discloses "re-evaluate the semaphore" (Page 2, Par. 0014)]**.

16. As per **claims 5 and 18**, the combination of Stone and Nieuwland discloses the method of claim 1, further comprising: writing an identification number, associated with a processor issuing the load with reservation instruction, into a status location associated with the addressed location in the shared memory when the data is accessed from the shared memory **[Stone discloses "plurality of processors (block 21)... each processor is composed of the blocks shown within block 21... The ResReg[j].S 34 field is typically a 1-bit status flag that indicates whether or not the reservation register 30 holds a reservation... the shared memory location 28 is associated with the register when the location 28 address is stored in the reservation register 30 ResReg[j]." (Col. 8, line 28-Col. 9, lines 3-6; Figure 1 and related text)]**.

17. As per **claim 6**, the combination of Stone and Nieuwland discloses the method of claim 1, further comprising: causing a reservation lost bit in a status register of the processor to indicate that the reservation was lost when the data at the address in shared memory is modified **["the invalidate process... sets the S bit of the matching reservation register 0, and this will prevent the success of a current or subsequent Write-if-Reserved" (Col. 14, line 38-48)]**.

18. As per **claim 7**, the combination of Stone and Nieuwland discloses the method of claim 6, wherein the step of determining whether the reservation was lost includes polling the status register and determining that the reservation was lost when the reservation lost bit so indicates **["TEST RESERVATIONS" (Col. 12, lines 26-46). Nieuwland discloses polling the semaphore (Page 2, Par. 0014)]**.

19. As per **claims 13 and 22**, Stone discloses the system of claim 12, but does not explicitly disclose the details wherein the at least one processing unit is operable to enter a low power consumption mode if the data is not a predetermined value.

Stone does not explicitly disclose the details of "entering a low power consumption mode."

Nieuwland discloses "entering a low power consumption mode" as **["whenever a station has to wait for the availability of data or buffer space, respectively, it may poll the remote semaphore to see whether the status of the buffer has changed. To prevent the need for polling and the associated bus load and power waste, an interrupt is provided for the consuming (producing) station by the producing (consuming) station after it has changed its own semaphore... Generally, a station may go into low-power mode whenever it has to wait for completion of the accessing by another station. Receiving an interrupt will wake up the idle station and will cause it to re-evaluate the semaphore that had caused the idle state" (Page 2, Par. 0014)]**.

Stone et al. (US 5,742,785) in view of Nieuwland et al. (US 2002/0083276) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the shared memory system which waits to receive a write privilege in order to write into a reserved register as taught by Stone and further have the waiting processor "entering a low power consumption mode" as taught by Nieuwland.

The motivation for doing so would have been because Nieuwland discloses entering a low power consumption mode is done to **[save power (Page 2, Par. 0014)]**.

Therefore, it would have been obvious to combine Stone et al. (US 5,742,785) with Nieuwland et al. (US 2002/0083276) for the benefit of creating a shared memory system to obtain the invention as specified in claims 13 and 22.

20. As per **claim 14**, the combination of Stone and Nieuwland discloses the system of claim 13, wherein the at least one processing unit is further operable to exit the low power consumption mode in response to an event that is permitted to interrupt the low power consumption mode **[Page 2, Par. 0014]**.

21. As per **claims 15**, the combination of Stone and Nieuwland discloses the system of claim 14, wherein the at least one processing unit is further operable to poll the one or more bits of the status register to determine whether the reservation was lost **[The rationale in the rejection to claim 7 is herein incorporated]**.

22. As per **claim 16**, the combination of Stone and Nieuwland discloses the system of claim 15, wherein the at least one processing unit is further operable to (i) re-instruct the memory interface unit to load the data with reservation from the shared memory at the specified address such that any operations may be performed on the data **[The rationale in the rejection to claims 4 and 11 is herein incorporated]**.

23. As per **claim 17**, the combination of Stone and Nieuwland discloses the system of claim 14, wherein the event that is permitted to interrupt the low power consumption mode is that the reservation was lost **[The rationale in the rejection to claims 2 and 9 is herein incorporated]**.

24. As per **claim 23**, the combination of Stone and Nieuwland discloses the system of claim 21, wherein the at least one processing unit is further operable to at least one of (i) exit the low power consumption mode, and (ii) suspend the other processing task, in response to an indication that the reservation was lost **[Stone discloses "if an invalidate request 104 is received, the invalidate is performed immediately" (Col. 14, lines 8-10) wherein "the invalidate process appears... it sets the S bit of the matching reservation register to 0, and this will prevent the success of a current or subsequent Write-If-Reserved instruction. The invalidate signifies that a variable has changed value or will change value in the immediate future" (Col. 14, lines 38-48). Nieuwland (Page 2, Par. 0014)]**.

25. As per **claims 24 and 25**, the combination of Stone and Nieuwland discloses the system of claim 21, wherein the at least one processing unit includes a status register having one or more bits indicating whether a reservation was lost, the reservation being lost when the data at the specified address in shared memory is modified; wherein the memory interface unit is operable to cause the one or more bits of the status register of the at least one processing unit to indicate that the reservation was lost **[Stone discloses "plurality of processors (block 21)... each processor is composed of the blocks shown within block 21... The ResReg[j].S 34 field is typically a 1-bit status flag that indicates whether or not the reservation register 30 holds a reservation... the shared memory location 28 is associated with the register when the**

location 28 address is stored in the reservation register 30 ResReg[j]." (Col. 8, line 28-Col. 9, lines 3-6; Figure 1 and related text)].

26. As per **claim 26**, the combination of Stone and Nieuwland the system of claim 24, wherein the at least one processing unit is further operable to poll the one or more bits of the status register to determine whether the reservation was lost **[The rationale in the rejection to claim 7 is herein incorporated]**.

27. As per **claim 27**, the combination of Stone and Nieuwland discloses the system of claim 25, wherein the at least one processing unit is further operable to (i) re-instruct the memory interface unit to load the data with reservation from the shared memory at the specified address such that any operations may be performed on the data **[The rationale in the rejection to claims 4 and 11 is herein incorporated]**.

28. As per **claim 28**, the combination of Stone and Nieuwland discloses the system of claim 21, wherein the memory interface unit is operable to write an identification number, associated with the at least one processing unit issuing the load with reservation instruction, into a status location associated with the specified address of the shared memory when the data is accessed from the shared memory **[The rationale in the rejection to claims 5 and 18 is herein incorporated]**.

29. **Claim 29** is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. (US 5,742,785) in view of Nieuwland et al. (US 2002/0083276) and Higuchi et al. (6,502,136).

30. As per **claim 29**, Stone discloses

A system, comprising: a shared memory; **["shared memory locations 28" (Figure 1)]**

a memory interface unit operatively coupled to the shared memory; and a plurality of N processing units in communication with the memory interface, the processing units being operable to execute a plurality of tasks in parallel **["interconnection network 20" (Figure 1 and related text) "read the share-memory locations, modify their contents, and then write back the new values atomically" (Col. 6, lines 54-62) "plurality of processors (block 21) (Col. 8, line 28-Col. 9, lines 3-6; Figure 1 and related text) "parallel processing environment" (Col. 8, line 38)]**.

a) performing one of the plurality of tasks; **["load with reservation" (Col. 9, line 54-Col. 10, line 35)]**

b) initializing a local variable, w; c) issuing a load with reservation instruction to the memory interface unit to load a shared variable, s, from the shared memory into the local variable w; d) incrementing or decrementing the local variable w toward the value of N; e) issuing a store conditionally instruction to the memory interface unit to facilitate storage of the value of the local variable w as the shared variable s in the shared memory; **["Load-with-Reservation" (Col. 9, line 54-Col. 10, line 35) "store contingent (sc): This instruction places a modified result value in a field of a reservation register associated with a shared memory location in preparation for an atomic update" (Col. 9, lines 57-60) "Write-if-reserved (WR): This instruction performs the atomic update of share memory locations whose addresses are held in reservation registers with valid contents, that have been updated by a Store Contingent instruction after placing the reservation. The atomic update occurs provided that all reservations are valid and write privilege has been obtained successfully for all reservations" (Col. 9, line 62-Col. 10, line 1)]**

f) repeating steps a)-e) if the reservation is lost, the reservation being lost when the shared variable at the address in shared memory is modified; **[Stone discloses "a message from a remote processor can arrive and invalidate a selected reservation. Therefore, the selected reservations are tested repeatedly" (Col. 12, lines 43-46)]**

g) issuing a store instruction to the memory interface unit to facilitate storage of a target value as the shared variable s in the shared memory when the value of the local variable reaches N; h) issuing a load with reservation instruction to the memory interface unit to load the shared variable s from the shared memory into the local variable w; **["The write-if-reserved instruction checks to confirm that the reservations held in specified registers remain valid, if so, it updates those shared variables whose reservation status registers show that the local copy of that variable has been modified" (Col. 7, lines 23-40); Col. 9, line 51-Col. 10, line 35)]**

i) entering a low power consumption mode, or initiating another processing task, when the value of the local variable is not the target value otherwise skip to step k); **["Write-if-reserved (WR): This instruction performs the atomic update of share memory locations whose addresses are held in reservation registers with valid contents, that have been updated by a Store Contingent instruction after placing the reservation. The atomic update occurs provided that all reservations are valid and write privilege has been obtained successfully for all reservations" (Col. 9, line 62-Col. 10, line 1)]**

j) exiting the low power consumption mode, or suspending the other processing task, and repeat steps h)-i) upon receipt of notification that the reservation was lost, the reservation being lost when a request for the shared variable in the shared memory is made by another processor;

[Stone discloses "a message from a remote processor can arrive and invalidate a selected reservation. Therefore, the selected reservations are tested repeatedly" (Col. 12, lines 43-46)]

and k) performing a next one of the plurality of tasks **[atomically updating shared variables (Col. 8, line 28-Col. 10, line 55)]**.

Stone does not explicitly disclose the details of "using barrier synchronization" or using a low power consumption mode.

Higuchi discloses barrier synchronization **[(Col. 25, lines 44-67; Col. 32, lines 41-58)]**.

Nieuwland discloses "entering a low power consumption mode" as **["whenever a station has to wait for the availability of data or buffer space, respectively, it may poll the remote semaphore to see whether the status of the buffer has changed. To prevent the need for polling and the associated bus load and power waste, an interrupt is provided for the consuming (producing) station by the producing (consuming) station after it has changed its own semaphore... Generally, a station may go into low-power mode whenever it has to wait for completion of the accessing by another station. Receiving an interrupt will wake up the idle station and will cause it to re-evaluate the semaphore that had caused the idle state" (Page 2, Par. 0014)]**.

Stone et al. (US 5,742,785) in view of Nieuwland et al. (US 2002/0083276) and Higuchi et al. (US 6,502,136) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the shared memory system which waits to receive a write privilege in order to

write into a reserved register as taught by Stone and further have the waiting processor, use barrier synchronization as disclosed by Higuchi and further "entering a low power consumption mode" as taught by Nieuwland.

The motivation for doing so would have been because Higuchi discloses a shared memory system that uses barrier synchronization in order to provide **[high speed operation between processing units (Col. 1, line 59-62)]** and Nieuwland discloses entering a low power consumption mode is done to **[save power (Page 2, Par. 0014)]**.

Therefore, it would have been obvious to combine Stone et al. (US 5,742,785) with Nieuwland et al. (US 2002/0083276) and Higuchi et al. (US 6,502,136) for the benefit of creating a shared memory system to obtain the invention as specified in claim 29.

RELEVANT ART CITED BY THE EXAMINER

31. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

32. The following references teach barrier synchronization.

US 5,796,946

US 5,983,326

US 5,566,321

33. The following reference teaches using a low power consumption mode.

US 2002/0013872

CLOSING COMMENTS

Examiner's Note

34. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

35. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

36. Per the instant office action, claims 1-29 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

38. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 12, 2007

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100